

**What is claimed is :**

1. A semiconductor device comprising a semiconductor layer, which comprises a compound semiconductor using  $Ga_vAl_{1-v}$  (where,  $0 \leq v \leq 1$ ) as the main component of the Group III-elements and N as the main component of the Group V-elements, and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor device, a second metal layer is in contact with the first metal layer, and a third metal layer is in contact with the second metal layer;

said second metal layer comprises a metal material having a higher melting point than those of metal materials in said first metal layer and said third metal layer; and

said third metal layer comprises a metal having a lower resistivity than those of metal materials in said first metal material and said second metal material.

2. A semiconductor device according to claim 1, wherein said first metal layer comprises any metal material selected from a group comprising Ni, Pt, Pd,  $Ni_zSi_{1-z}$ ,  $Pt_zSi_{1-z}$ ,  $Pd_zSi_{1-z}$ ,  $Ni_zN_{1-z}$ , and  $Pd_zN_{1-z}$  (where,  $0 < z < 1$ ); and said second metal layer comprises any metal material selected from a group comprising Mo, Pt, W, Ti, Ta,  $Mo_xSi_{1-x}$ ,  $Pt_xSi_{1-x}$ ,  $W_xSi_{1-x}$ ,  $Ti_xSi_{1-x}$ ,  $Ta_xSi_{1-x}$ ,  $Mo_xN_{1-x}$ ,  $W_xN_{1-x}$ ,  $Ti_xN_{1-x}$ , and  $Ta_xN_{1-x}$  (where,  $0 < x < 1$ ).

3. A semiconductor device according to claim 2, wherein said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

4. A semiconductor device according to claim 1, wherein said first metal layer comprises any material selected from a group comprising  $Ni_{z1}Si_{1-z1}$  (where,  $0.4 \leq z1 \leq 0.75$ ),  $Pt_{z2}Si_{1-z2}$  (where,  $0.5 \leq z2 \leq 0.75$ ),  $Pd_{z3}Si_{1-z3}$  (where,  $0.5 \leq z3 \leq 0.85$ ),  $Ni_{z4}N_{1-z4}$  (where,  $0.5 \leq z4 \leq 0.85$ ), and  $Pd_{z5}N_{1-z5}$  (where,  $0.5 \leq z5 \leq 0.85$ ); and said second metal layer comprises any material selected from a group comprising any of Mo, Pt, W, Ti, Ta,  $Mo_xSi_{1-x}$ ,  $Pt_xSi_{1-x}$ ,  $W_xSi_{1-x}$ ,  $Ti_xSi_{1-x}$ ,  $Ta_xSi_{1-x}$ ,  $Mo_xN_{1-x}$ ,  $W_xN_{1-x}$ ,  $Ti_xN_{1-x}$ , and  $Ta_xN_{1-x}$  (where,  $0 < x < 1$ ).

5. A semiconductor device according to claim 4, wherein said third metal layer comprises any material selected from a group comprising any of Au, Cu, Al, and Pt.

6. A semiconductor device according to claim 1, wherein said first metal layer  
5 comprises a metal material having a higher work function than that of said second metal layer.

7. A semiconductor device according to claim 6, wherein said first metal layer  
10 comprises a metal material having a higher work function than that of said third metal layer.

8. A semiconductor device according to claim 1, wherein the melting point of said second metal layer is 1,000°C or higher.

9. A semiconductor device according to claim 1, wherein said semiconductor  
15 layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

10. A semiconductor device according to claim 9, wherein said substrate comprises  
20 any substrate selected from a group comprising a sapphire substrate, a SiC substrate and a GaN substrate.

11. A semiconductor device according to claim 1, wherein said semiconductor  
25 layer is an  $\text{Al}_u\text{Ga}_{1-u}\text{N}$  layer (where,  $0 \leq u \leq 1$ ).

12. A semiconductor device according to claim 1, wherein said semiconductor  
layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

13. A semiconductor device according to claim 12, wherein said GaN compound  
30 semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

14. A semiconductor device according to claim 1, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

5 15. A semiconductor device according to claim 14, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

10 16. A semiconductor device according to claim 1, wherein said semiconductor layer is a n-type GaN channel layer.

17. A semiconductor device comprising a semiconductor layer comprising a compound semiconductor using  $\text{Ga}_v\text{Al}_{1-v}$  (where,  $0 \leq v \leq 1$ ) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:  
 15 said Schottky junction metal layer comprises a laminated structure comprising a first metal layer which is in contact with said semiconductor layer and a second metal layer which is in contact with said first metal layer; and  
 20 said first metal layer comprises a metal material having a higher melting point than that of the metal material in said second metal layer and said second metal layer comprises a metal material having a lower resistivity than that in the metal material of said first metal layer.

25 18. A semiconductor device according to claim 17, wherein said first metal layer comprises any metal material selected from a group comprising  $\text{Ni}_y\text{Si}_{1-y}$ ,  $\text{Pt}_y\text{Si}_{1-y}$ ,  $\text{Pd}_y\text{Si}_{1-y}$ ,  $\text{Ni}_y\text{N}_{1-y}$ , and  $\text{Pd}_y\text{N}_{1-y}$  (where,  $0 < y < 1$ ).

30 19. A semiconductor device according to claim 18, wherein said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al and Pt.

20. A semiconductor device according to claim 17, wherein said first metal layer comprises any metal material selected from a group comprising  $\text{Ni}_{y1}\text{Si}_{1-y1}$  (where,  $0.4 \leq y1 \leq 0.75$ ),  $\text{Pt}_{y2}\text{Si}_{1-y2}$  (where,  $0.5 \leq y2 \leq 0.5$ ),  $\text{Pd}_{y3}\text{Si}_{1-y3}$  (where,  $0.5 \leq y3 \leq 0.85$ ),  
 35  $\text{Ni}_{y4}\text{N}_{1-y4}$  (where,  $0.5 \leq y4 \leq 0.85$ ), and  $\text{Pd}_{y5}\text{N}_{1-y5}$  (where,  $0.5 \leq y5 \leq 0.85$ ).

21. A semiconductor device according to claim 20, wherein said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

22. A semiconductor device according to claim 17, wherein said first metal layer  
5 has a higher work function than that of said second metal layer.

23. A semiconductor device according to claim 17, wherein the melting point of said first metal layer is 1,000°C or higher.

10 24. A semiconductor device according to claim 17, wherein said semiconductor layer is formed on a multilayered structure comprising a plurality of compound semiconductor layers formed on a substrate.

25. A semiconductor device according to claim 17, wherein said substrate  
15 comprises any substrate selected from a group comprising a sapphire substrate, a SiC substrate, and a GaN substrate.

26. A semiconductor according to claim 17, wherein said semiconductor layer is an  $\text{Al}_u\text{Ga}_{1-u}\text{N}$  layer (where,  $0 \leq u \leq 1$ ).  
20

27. A semiconductor device according to claim 17, wherein said semiconductor layer is a GaN compound semiconductor electron supplying layer formed on a GaN compound semiconductor channel layer.

25 28. A semiconductor device according to claim 27, wherein said GaN compound semiconductor channel layer comprises a compound semiconductor selected from a group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

30 29. A semiconductor device according to claim 17, wherein said semiconductor layer is a GaN compound semiconductor channel layer formed on a GaN compound semiconductor electron supplying layer.

30. A semiconductor device according to claim 29, wherein said GaN compound  
35 semiconductor channel layer comprises a compound semiconductor selected from a

group comprising GaN and InGaN, and said GaN compound semiconductor electron supplying layer comprises AlGaN.

31. A semiconductor device according to claim 17, wherein said semiconductor layer is a n-type GaN channel layer.

32. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using  $\text{Ga}_v\text{Al}_{1-v}$  (where,  $0 \leq v \leq 1$ ) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:  
 said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer, a second metal layer is in contact with said first metal layer, and a third metal layer is in contact with said second metal layer;  
 said first metal layer comprises any metal material selected from a group comprising Ni, Pt, Pd,  $\text{Ni}_z\text{Si}_{1-z}$ ,  $\text{Pt}_z\text{Si}_{1-z}$ ,  $\text{Pd}_z\text{Si}_{1-z}$ ,  $\text{Ni}_z\text{N}_{1-z}$ , and  $\text{Pd}_z\text{N}_{1-z}$  (where,  $0 < z < 1$ );  
 said second metal layer comprises any metal material selected from a group comprising Mo, Pt, W, Ti, Ta,  $\text{Mo}_x\text{Si}_{1-x}$ ,  $\text{Pt}_x\text{Si}_{1-x}$ ,  $\text{W}_x\text{Si}_{1-x}$ ,  $\text{Ti}_x\text{Si}_{1-x}$ ,  $\text{Ta}_x\text{Si}_{1-x}$ ,  $\text{Mo}_x\text{N}_{1-x}$ ,  $\text{W}_x\text{N}_{1-x}$ ,  $\text{Ti}_x\text{N}_{1-x}$ , and  $\text{Ta}_x\text{N}_{1-x}$  (where,  $0 < x < 1$ ); and  
 said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

33. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using  $\text{Ga}_v\text{Al}_{1-v}$  (where,  $0 \leq v \leq 1$ ) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:  
 said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;  
 said first metal layer comprises any metal material selected from a group comprising  $\text{Ni}_y\text{Si}_{1-y}$ ,  $\text{Pt}_y\text{Si}_{1-y}$ ,  $\text{Pd}_y\text{Si}_{1-y}$ ,  $\text{Ni}_y\text{N}_{1-y}$ , and  $\text{Pd}_y\text{N}_{1-y}$  (where,  $0 < y < 1$ ); and  
 said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

34. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using  $\text{Ga}_v\text{Al}_{1-v}$  (where,  $0 \leq v \leq 1$ ) as a main component of the

Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein:

said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer and a third metal layer is in contact with said metal layer;

said first metal layer comprises any metal material selected from a group comprising  $\text{Ni}_{z1}\text{Si}_{1-z1}$  (where,  $0.4 \leq z1 \leq 0.75$ ),  $\text{Pt}_{z2}\text{Si}_{1-z2}$  (where,  $0.5 \leq z2 \leq 0.75$ ),  $\text{Pd}_{z3}\text{Si}_{1-z3}$  (where,  $0.5 \leq z3 \leq 0.85$ ),  $\text{Ni}_{z4}\text{N}_{1-z4}$  (where,  $0.5 \leq z4 \leq 0.85$ ), and  $\text{Pd}_{z5}\text{N}_{1-z5}$  (where,  $0.5 \leq z5 \leq 0.85$ );

said second metal layer comprises any metal material selected from a group comprising Mo, Pt, W, Ti, Ta,  $\text{Mo}_x\text{Si}_{1-x}$ ,  $\text{Pt}_x\text{Si}_{1-x}$ ,  $\text{W}_x\text{Si}_{1-x}$ ,  $\text{Ti}_x\text{Si}_{1-x}$ ,  $\text{Ta}_x\text{Si}_{1-x}$ ,  $\text{Mo}_x\text{N}_{1-x}$ ,  $\text{W}_x\text{N}_{1-x}$ ,  $\text{Ti}_x\text{N}_{1-x}$ , and  $\text{Ta}_x\text{N}_{1-x}$  (where,  $0 < x < 1$ ); and

said third metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.

35. A semiconductor device comprising a semiconductor layer which comprises a compound semiconductor using  $\text{Ga}_v\text{Al}_{1-v}$  (where,  $0 \leq v \leq 1$ ) as a main component of the Group III-elements and N as a main component of the Group V-elements and a Schottky junction metal layer which is in contact with the semiconductor layer, wherein said Schottky junction metal layer comprises a laminated structure wherein a first metal layer is in contact with said semiconductor layer and a second metal layer is in contact with said first metal layer;

said first metal layer comprises any metal material selected from a group comprising  $\text{Ni}_{y1}\text{Si}_{1-y1}$  (where,  $0.4 \leq y1 \leq 0.75$ ),  $\text{Pt}_{y2}\text{Si}_{1-y2}$  (where,  $0.5 \leq y2 \leq 0.75$ ),  $\text{Pd}_{y3}\text{Si}_{1-y3}$  (where,  $0.5 \leq y3 \leq 0.85$ ),  $\text{Ni}_{y4}\text{N}_{1-y4}$  (where,  $0.5 \leq y4 \leq 0.85$ ), and  $\text{Pd}_{y5}\text{N}_{1-y5}$  (where,  $0.5 \leq y5 \leq 0.85$ ); and

said second metal layer comprises any metal material selected from a group comprising Au, Cu, Al, and Pt.